

REMARKS

I. General

Claims 1-3, 6-13, and 16-19 are pending in the application, and all are rejected by the Office Action, mailed June 30, 2004. Claims 1-3, 6-13, and 16-18 are indicated as allowable over the cited art of record. Claim 19 is amended. The issues in the current Office Action are as follows:

- The specification is objected to.
- Claims 1-3, 6-13, and 16-19 are provisionally rejected under the judicially created doctrine of double patenting over claims 1-3, 5-13, and 15-18 of copending application 09/510,128.
- Claim 19 is rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent 6,453,387 (hereinafter, *Lozano*).
- Claim 19 is also rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent 5,809,528 (hereinafter, *Miller*).

Applicants hereby traverse the outstanding rejections and request reconsideration and withdrawal in light of the remarks contained herein.

II. Amendments

Claim 19 is amended to recite, in part, “a force update command for causing said plurality of entry locations to acquire predetermined illegal bit values.” Support may be found at least at page 9, lines 6-10 of the present specification. Thus, no new matter is added.

III. Objection to the Specification

The specification is objected to for informalities. Specifically, the Examiner requests that updated status information about the incorporated patents be provided. Applicants have amended the specification to update those statuses and respectfully request withdrawal of the objection.

IV. Double Patenting Rejection

Claims 1-3, 6-13, and 16-19 stand provisionally rejected under the judicially created doctrine of double patenting over claims 1-3, 5-13, and 15-18 of copending application 09/510,128. Applicants propose filing a terminal disclaimer in compliance with 37 C.F.R. 1.321(b) if the Examiner's rejections still stand upon indication that the claims of the present application are otherwise allowable.

V. Rejections Under 35 U.S.C. §102**A. Rejections over Lozano**

On page 3 of the Office Action, claim 19 is rejected under 35 U.S.C. §102(e) as being anticipated by *Lozano*. To anticipate a claim under 35 U.S.C. § 102, a reference must teach every element of the claim, see M.P.E.P. § 2131. Moreover, in order for an applied reference to be anticipatory under 35 U.S.C. § 102 with respect to a claim, “[t]he identical invention must be shown in as complete detail as is contained in the . . . claim,” see M.P.E.P. § 2131, citing *Richardson v. Suzuki Motor Co.*, 9 U.S.P.Q.2d 1913 (Fed. Cir. 1989). As discussed further below, these requirements are not satisfied by the 35 U.S.C. §102 rejection of claim 19 because *Lozano* does not teach every element of that claim.

Claim 19 recites, in part, “a force update command for causing said plurality of entry locations to acquire predetermined . . . bit values not present in prospective entries at ports connected to said fully associative table.”

Applicants respectfully assert that *Lozano* does not teach at least the above recited feature of claim 19. The Office Action cites Col. 9, lines 40-55; however, the cited passage from *Lozano* simply illustrates that the memory device in *Lozano* enters new addresses into the tag portion of the memory unit. The system of *Lozano* performs that operation whenever the memory unit encounters an address that is not already a valid memory address. See Col. 9, lines 33-41. Therefore, *Lozano* does not teach storing values in a table in a way other than in the normal course of operation of the system, and therefore, does not teach using a force command to cause entry locations to acquire predetermined bit values not present in prospective entries. Thus, claim 19 is patentable over *Lozano*. Accordingly, Applicants respectfully request withdrawal of the 35 U.S.C. §102(e) rejection of claim 19.

B. Rejections over Miller

On page 4 of the Office Action, claim 19 is rejected under 35 U.S.C. §102(b) as being anticipated by *Miller*. Amended claim 19 recites, in part, “a force update command for causing said plurality of entry locations to acquire predetermined illegal bit values not present in prospective entries at ports connected to said fully associative table.” Applicants assert that *Miller* does not teach at least the above recited feature of claim 19. The Office Action cites Col. 15, lines 35-50; however that passage teaches that, at initialization, all valid status bits are set to an invalid state. The passage does not teach illegal bit values, but rather, teaches invalid bit values.

The current specification at page 8, lines 22-23 defines “illegal value” to refer to a value which a prospective entry would preferably not acquire in a normal course of program execution. The invalid values referred to in *Miller* are values that are stored but are no longer current. See Col. 3, lines 13-24. That same passage teaches that data becomes old (not current) during the normal course of execution of a multi-processor system. Therefore, the invalid bits of *Miller* are not the same as the illegal bit values of claim 19. Because *Miller* does not teach values which a prospective entry would preferably not acquire in a normal course of program execution, it does not teach the above recited feature of claim 19. Thus, claim 19 is patentable over *Miller*. Accordingly, Applicants respectfully request withdrawal of the 35 U.S.C. §102(b) rejection of claim 19.

VI. Conclusion

In view of the above amendment and arguments, Applicants believe the pending application is in condition for allowance.

Application No.: 10/687,907

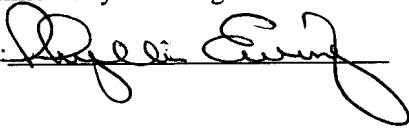
Docket No.: 10971353-3

Applicants believe no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 08-2025, under Order No. 10971353-3 from which the undersigned is authorized to draw.

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